Amendments to the Specification

Please amend the specification as indicated.

Please insert the following after line 2 on page 1:

CROSS-REFERENCE TO RELATED APPLICATIONS

Please amend the paragraph inserted on page 1 between lines 3 and 4 (in the Preliminary Amendment filed on September 15, 2000) as follows:

This application is a continuation of U.S. Patent Application No. 09/263,798, filed March 5, 1999, now U.S. Patent No. 6,266,758 B1, issued July 24, 2001, which is a continuation of U.S. Patent Application No. 08/947,649, filed October 9, 1997, now U.S. Patent No. 5,933,650, issued August 3, 1999.

Please amend the paragraph starting on page 15, line 26, as follows:

In one embodiment of the present invention, an alignment instruction provides an immediate, which is a constant byte address within a doubleword. Preferably, the immediate consists of 3 bits for specifying a constant byte address to a byte among 8 bytes each in the first register (i.e., little-endian mode processor) and the second register (i.e., ~~bit-endian~~ big-endian mode processor). This alignment instruction performs a constant alignment of a vector. The align amount is computed by masking the immediate, then using that value to control a funnel shift of vector vs concatenated with vector vt. The operands can be in the QH, OB, or BW format.